CLAIMS

What is claimed is:

1. An apparatus for inhibiting data cache thrashing in a multi-threading execution mode through simulating a higher level of associativity in a data cache, comprising:

at least one instruction register, the at least one instruction register having a thread ID indicator;

an address generator having a cache index indicator and a plurality of cache index bits;

a cache memory; and

a selector for selecting between the thread ID indicator and the cache index indicator, the selector outputting an upper index indicator,

wherein when the thread ID indicator is selected by the selector, the thread ID indicator is output to the upper index indicator, and the upper index indicator is concatenated with the plurality of cache index bits to form an address for retrieving an entry from the cache memory.

2. The apparatus of claim 1, further comprising a machine state register, the machine state register having an enable cache split indicator that, at least, controls the selector.

3. The apparatus of claim 1, further comprising at least one cache miss counter, the at least one cache miss counter counting cache misses, wherein the at least one cache miss counter controls the selector.

4. The apparatus of claim 1, wherein each thread ID indicator further comprises a plurality of bits.

5. The apparatus of claim 1, wherein each thread ID indicator further comprises a single bit.

6. A method for inhibiting data cache thrashing in a multi-threading execution mode through simulating a higher level of associativity in a data cache, comprising the steps of:

loading at least one instruction register, the at least one instruction register having a thread ID indicator;

generating an effective address having a cache index indicator and a plurality of cache index bits;

selecting an upper index indictor between the thread ID indicator and the cache index indicator;

forming an address by concatenating the upper index indicator with the plurality of cache index bits; and

retrieving an entry from the cache memory indicated by the address.

7. The method of claim 6, wherein the step of selecting an upper index indicator further comprises the steps of:

checking an enable cache indicator in a machine state register;

if the enable cache indicator is set, selecting the thread ID bit; and

if the enable cache indicator is not set, selecting the cache index indicator.

8. The method of claim 6, wherein the step of selecting an upper index indicator further comprises the steps of:

counting cache misses;

if the number of cache misses exceeds a predefined limit, selecting the thread ID bit; and

if the number of cache misses is less than the predefined limit, selecting the cache index indicator.

9. The method of claim 6, wherein each instruction register further comprises a stream ID indicator, wherein the step of selecting an upper index indicator further comprises the steps of:

checking a valid indicator and the stream ID indicator of the at least one instruction register; and

if at least one instruction register having both the valid indicator and the stream ID indicator set, selecting the thread ID bit.

10. An apparatus for inhibiting data cache thrashing in a multi-threading execution mode through simulating a higher level of associativity in a data cache, comprising:

a first means for storing instruction having a thread ID indicator;

a second means for generating addresses having a cache index indicator and a plurality of cache index bits;

a third means for storing data; and

a fourth means for selecting between the thread ID indicator and the cache index indicator, the fourth means having an upper index indicator,

wherein when the thread ID indicator is set and selected by the fourth means, the thread ID indicator is connected to the upper index indicator, and the upper index indicator is concatenated with the plurality of cache index bits to form an address to retrieve an entry from the third means.